Active Matrix

Flat Panel Displays

Part 1. LCD (2)

Active Matrix Addressing

Active matrix addressing is shown schematically in Fig. 4.5a, in which the plate is patterned into an array of pixels, each one of which is addressed by its own transistor.

→ The most widely used addressing transistor is an a-Si:H TFT: this is shown in the pixel layout in Fig. 4.5b, and in cross-section in Fig. 4.5c

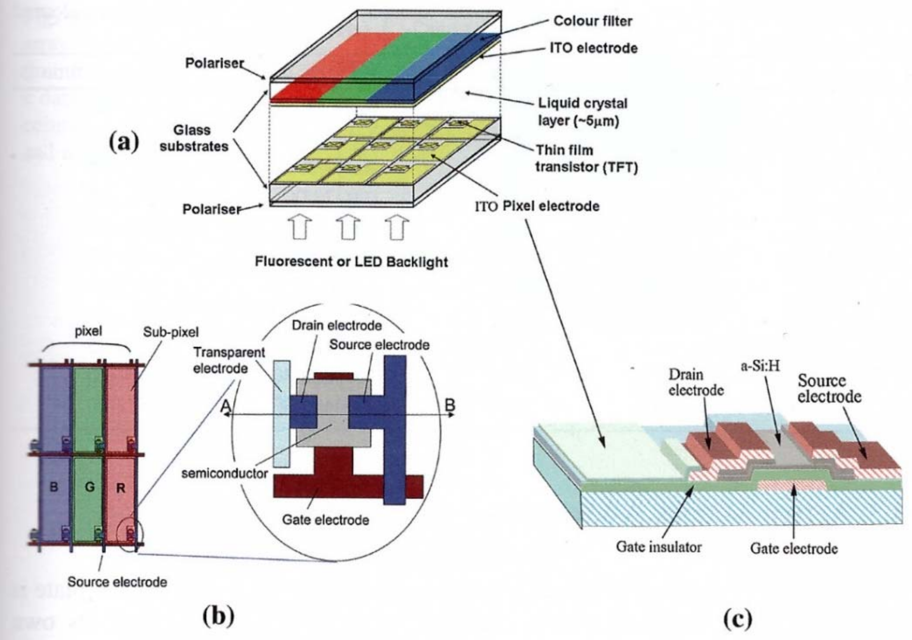


Fig. 4.5 **a** Illustration of AMLCD cell, **b** detail of pixel layout, showing TFT, **c** schematic cross-section of a-Si:H TFT (**b** and **c** reprinted with permission from [19])

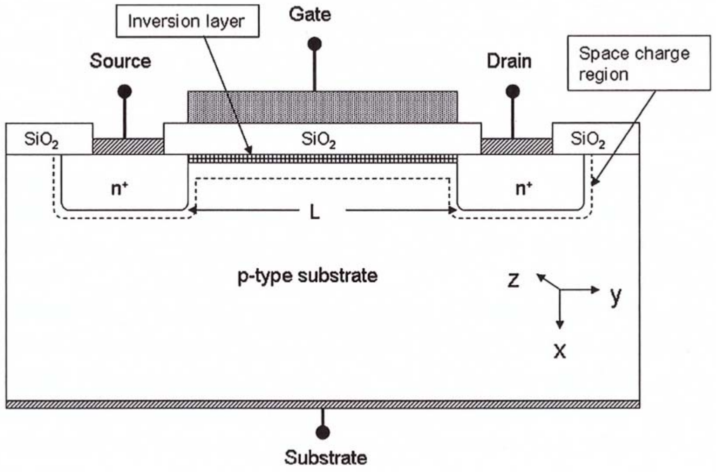


Fig. 3.1 Schematic cross section of a MOSFET, with the gate voltage larger than the threshold voltage, and showing the surface inversion and depletion layers. The channel length is L, and the width, W, is perpendicular to the page

Although this is a field-effect transistor, like the MOSFET discussed previously, its architecture is quite different, being a bottom-gated inverted staggered structure, rather than a top-gated coplanar structure.

Moreover, the source and drain connections are not self-aligned to the gate electrode, but overlap it.

This overlap results in a parasitic capacitance, C_{GD}, between the gate and the drain terminals, which can induce display performance artefacts.

→ In the MOSFET case, the edges of the source and drain regions are coincident with the gate edges, which is the standard MOSFET architecture.

This architecture is referred to as self-aligned, and is achieved by using the gate electrode as a mask for doping the source and drain regions by ion implantation.

As illustrated in Fig. 4.6a, the matrix of TFTs is connected in rows and columns, with a common connection to the gate electrodes in each row, and a common connection to the source terminals in each column.

→ The row lines carry the TFT addressing signals, and the column lines carry the data signal, V_s.

→ The drain of each TFT is connected to its ITO pixel electrode, and the timing of the row and column voltages are shown in Fig. 4.6b and c, respectively.

→ The high resistivity LC material is represented by a capacitor, which is charged up to the appropriate signal voltage, V_s, through its TFT.

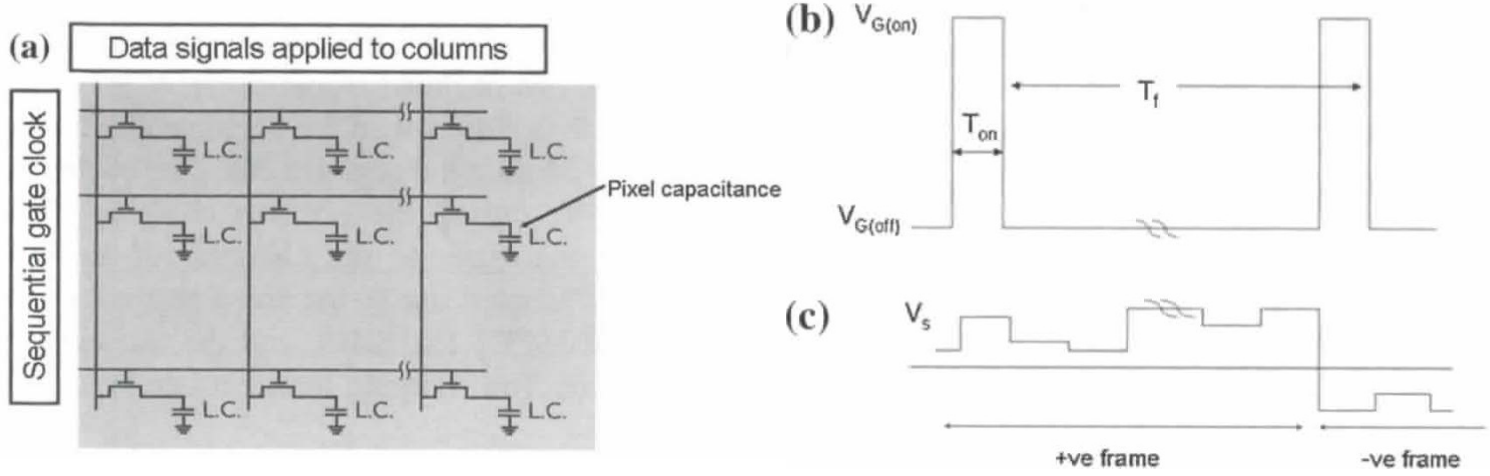


Fig. 4.6 **a** Active matrix array layout, **b** Gate line timing signal for row m, and **c** data signal waveform for column n, showing positive and negative frames

This is achieved by line-at-a-time addressing, during which the data signal is fed into the display in a serial row-by-row process, by sequentially switching on each row ($V_G = V_{G(on)}$), whilst holding the others in the off-state ($V_G = V_{G(off)}$).

→ If the addressing TFTs are made from a-Si:H, they will be n-channel devices, and the row select voltages, $V_{G(on)}$, will be positive, whilst the row de-select voltage, $V_{G(off)}$, will be negative.

→ The timing signals are related to the a.c. mains frequency, such that the display is refreshed every frame time, T_f, which will be 16.7 ms (1/60) for a 60 Hz frame rate.

If there are M rows and N columns in the display, then the time available, T_{on}, to charge the TFTs in a given row is given by T_f/M, and this will be a function of the display format.

Table 4.1 lists the row addressing times, which vary from ~35 to ~7 μs, across the range of display formats.

During this interval, the signal voltages on the column electrodes of the display are applied in parallel to the common sources of the TFTs, but will charge only the one row of LC capacitors connected to the row of TFTs, which has been turned on.

→ The on-current of the TFTs must be large enough to charge the capacitors in the time available.

The maximum charge will be when the voltage is changing from +black to –black, i.e., $+V_{sat}$ to $-V_{sat}$ (or vice versa), and an approximate value of the required current is given by:

$$I_{on} > 5 \times \frac{2V_{sat}C_{LC}}{T_{on}} \rightarrow \text{(for example, } I_{on} \geq 3.6 \times 10^{-7} A \text{ for } C_{LC} = 0.25\, pF\text{)} \quad (1)$$

where C_{LC} is the capacitance of the LC, and the factor 5 is to ensure the full charging of the pixel.

At the end of the row on-time, that row is deselected (by switching the gate bias to a negative value), and the adjacent row is switched on, and the process described above is repeated.

→ Hence, the display information is loaded row by row during a frame time, and, at the end of this period, the whole process is repeated with the next ‘field’ of information.

→ However, between the loading of the data signals onto a given row of TFTs, and its updating a frame-rate later, it is important that the original signal voltages are maintained across the LC capacitor.

During this interval, the sources of the de-selected TFTs will experience a variety of different voltages, which will be different from the voltage, V_{LC}, on the drain terminal, and, depending upon the TFT leakage current, this potential difference acts as a driving force to reset the voltage on the drain.

To ensure that this effect is minimized, the maximum tolerable leakage current, I_{off}, is constrained to be below a certain maximum value, to give, for instance, less than 1% discharge of the pixel voltage, so that:

$2V_{sat}$

$$I_{off} < 10^{-2} \times \frac{C_{LC}\Delta V_{max}}{T_f} \rightarrow \text{(for example, } I_{off} \leq 4.5 \times 10^{-13} A \text{ for } C_{LC} = 0.25\ pF\text{)} \tag{2}$$

→ Hence, with line-at-a-time addressing, the TFT is acting as a high quality switch, with a minimum on:off current ratio given by Eqs. (1) and (2)

$$\frac{I_{on}}{I_{off}} > 500M > 5 \times 10^5 \text{ for a display with ~1000 rows}$$

rows

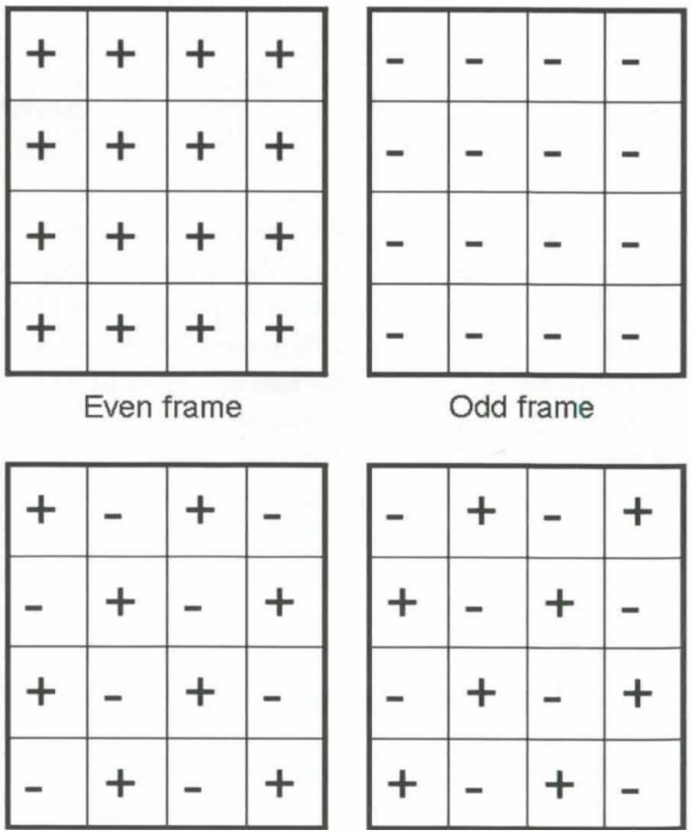
The other potential leakage current path is through the LC itself, but its resistivity is typically ~$1 \times 10^{12} \Omega \cdot cm$, and, although this is not negligible, the associated leakage will be less than the TFT leakage.

The polarity of the signal voltages is changed in a uniform fashion across the whole field between frames. (polarity inversion)

→ This is illustrated in Fig. 4.8a, and is known as frame inversion.

From a display performance point of view, this has well documented drawbacks, such as increased flicker, and increased vertical cross-talk.

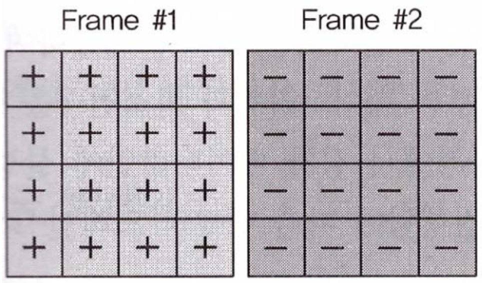
Fig. 4.8 AMLCD data signal drive inversion schemes, showing the signal polarity in consecutive frames with (**a**) frame inversion, and (**b**) dot inversion



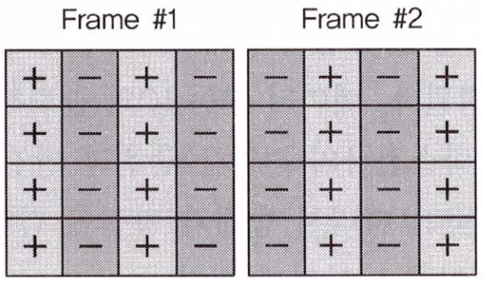
→ In fact, there are several alternative inversion schemes, such as row inversion (the polarity of each row of data alternates within one frame), or column inversion (the polarity of each column of data alternates within one frame), or dot inversion.

Dot inversion is a mixture of row and column inversion, in which the polarity of every other pixel alternates, and gives the lowest value of cross-talk and flicker.

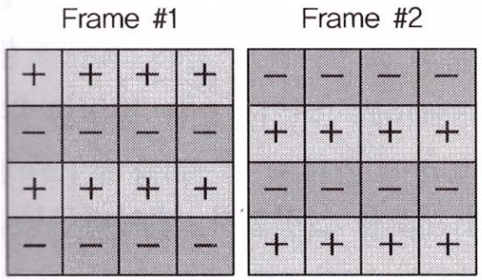
In all these schemes, the polarity pattern within one frame is reversed in the next frame, so that each LC pixel experiences alternating +ve and –ve biases.



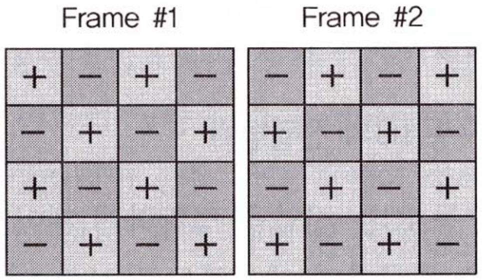
Frame Inversion



Column Inversion



Line Inversion



Dot Inversion

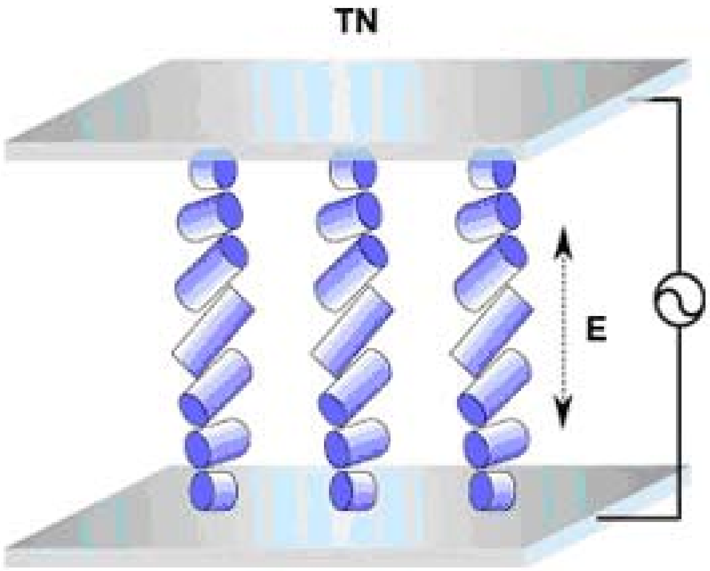
The foregoing description of active matrix addressing of LCDs is somewhat simplified and idealized, and there are important behavioral artefacts associated with parasitic capacitances within the pixel, such as cross-talk and pixel off-set voltage (=kick-back voltage).

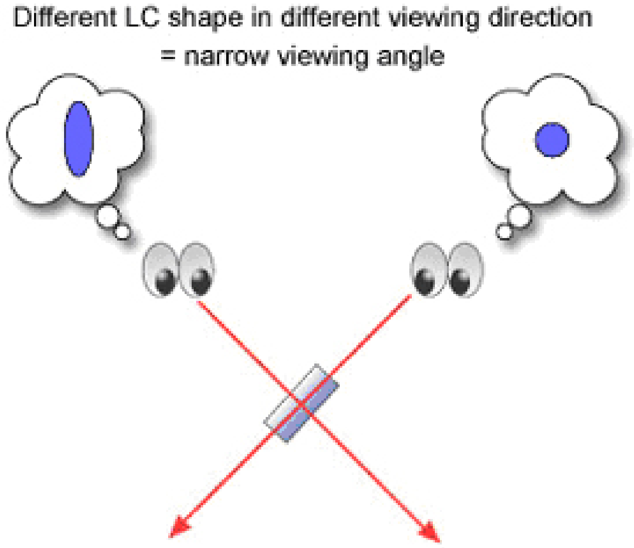
→ The magnitude of these effects is determined by the detailed pixel layout, and these effects will be discussed next.

It should also be mentioned that additional capacitance is frequently introduced in parallel with the pixel capacitance, by means of a storage capacitor.

Finally, the viewing angle dependence of brightness and contrast in the simple TN cell is limited, and, although it is acceptable in smaller displays up to notebook size, it was necessary to improve it in the larger monitor and TV displays.

→ In this TN cell, at mid-grey levels, the LC director is changing direction from horizontal towards vertical in the middle of the cell, and, at different viewing angles, this variable direction changes the transmittance of the cell.


TN


Different LC shape in different viewing direction
= narrow viewing angle

To improve the viewing angle, modified cell architecture have been developed, of which the two most widely used are the in-plane switching (IPS), and the multi-domain vertical alignment mode (VA).

→ The operation of the IPS cell, with crossed polarizers, is shown in the off and on states in Fig. 4.9a and b, respectively.

In both cases, the LC director is parallel to the plane of the glass plates (and in Fig. 4.9a, the director is perpendicular to the page).

The major difference from the simple TN cell, is that the switching electrodes are on the TFT plate, so that, when a bias is applied between these electrodes, the molecules rotate about their short axis, and the director aligns with the field.

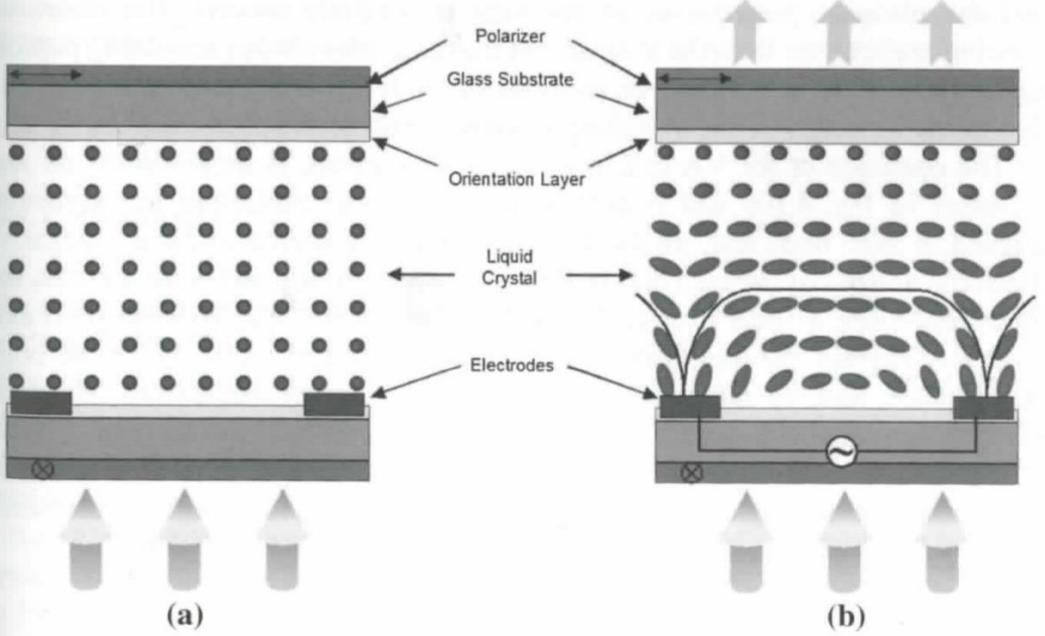


Fig. 4.9 Illustration of the normally black, IPS mode of LC cell switching. **a** Zero bias dark-state. **b** Biased bright-state (Reprinted from [10] with permission of SID)

This puts a twist into the column of liquid crystal molecules, and the plane of polarization of the light is similarly rotated.

The improved viewing angle arises from the long axis of the molecules always remaining parallel to the plane of the cell.

However, the trade-off with IPS is a reduced aperture ratio due to the inclusion of the switching electrodes within the pixel.

→ The operation of the VA cell, with crossed polarizers, is shown in the off and on-states in Fig. 4.10a and b, respectively.

The molecules are vertically aligned at zero bias, and, as the LC mixture is engineered to have a negative dielectric anisotropy, when a bias is applied between the top and bottom plates, the molecules rotate in order to align their short axis with the field.

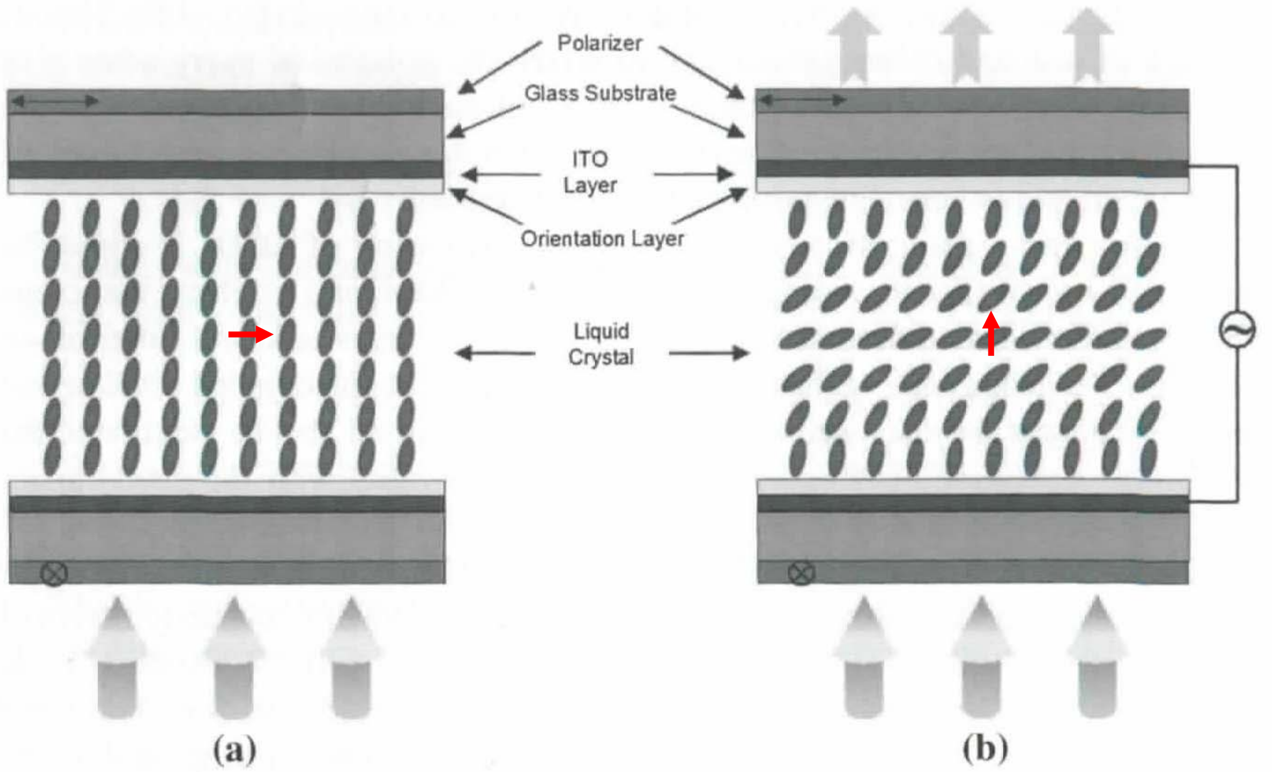
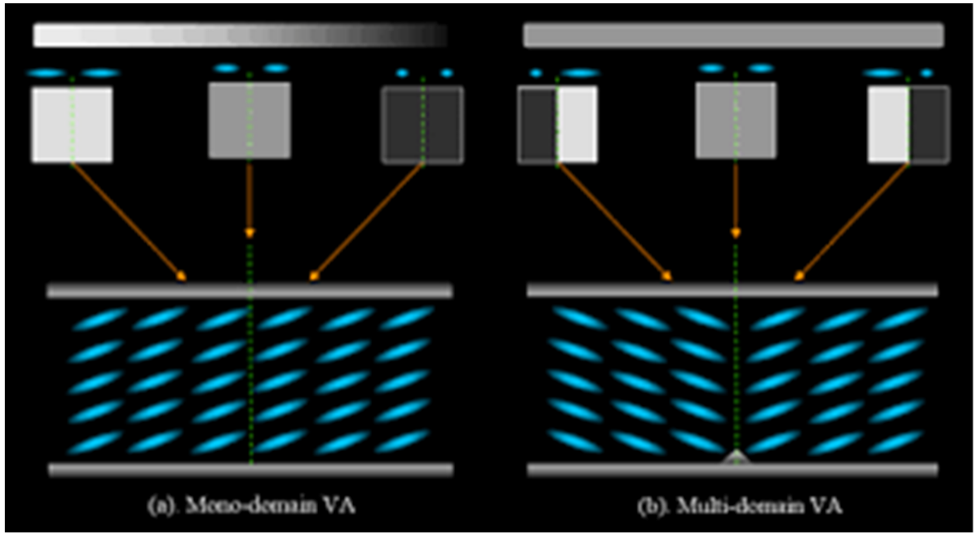


Fig. 4.10 Illustration of the normally black, VA mode of LC cell switching. **a** Zero bias dark-state. **b** Biased bright-state (Reprinted from [10] with permission of SID)

With the short axis vertically aligned, the long axis of the molecule is free to rotate within the horizontal plane, and, by sub-dividing and texturing the pixel surface, the long axis is constrained to lie in different directions within the sub-divided pixel.

Hence, in a pixel containing four sub-pixel domains, the same molecule orientation is seen from different angles, which greatly improves the viewing angle performance of the VA cell compared with conventional TN cell.



The average of the two is the same.

MVA: Multiple-Domain VA

PVA: Patterned VA (Samsung)