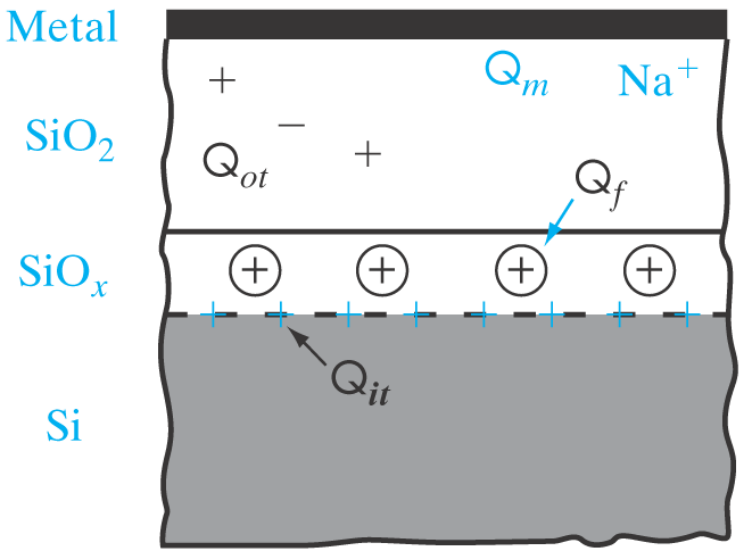
Oxide Charge-A Modification to V_{fb} and V_t



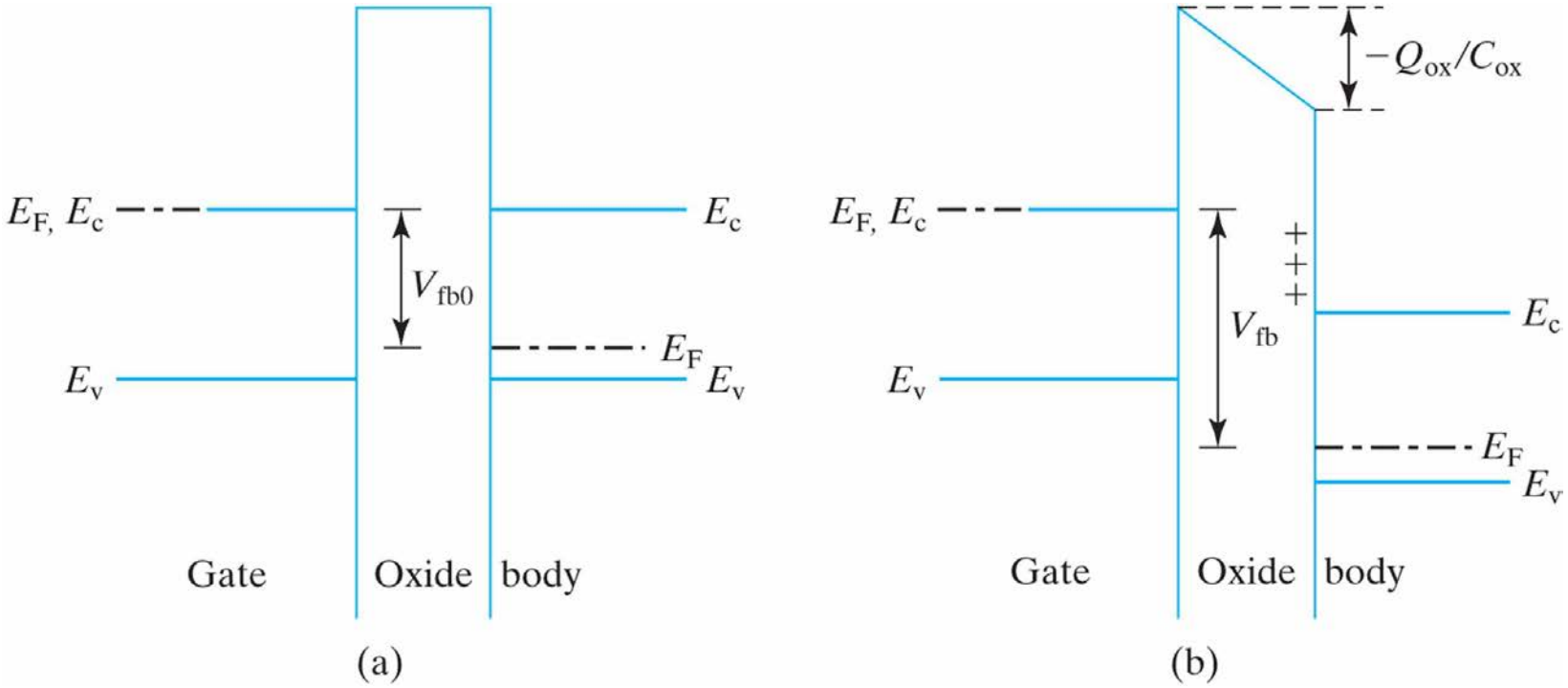
- **Q_m(mobile ionic charge);**
  cause instabilities in V_{fb} and V_t.
- **Q_{ot} (oxide trapped charge)**
- **Q_f (fixed oxide charge)**
- **Q_{it} (interface trapped charge);**
  degrade the substrate current of MOSFET.

Reliability

More Q_{it} and Q_f appear after the oxide is subjected to high field some time due to the breaking or rearrangement of chemical bonds

This raises a reliability concern because the V_t.

Oxide Charge-A Modification to V_{fb} and V_t



Flat-band condition (no band bending at body surface)

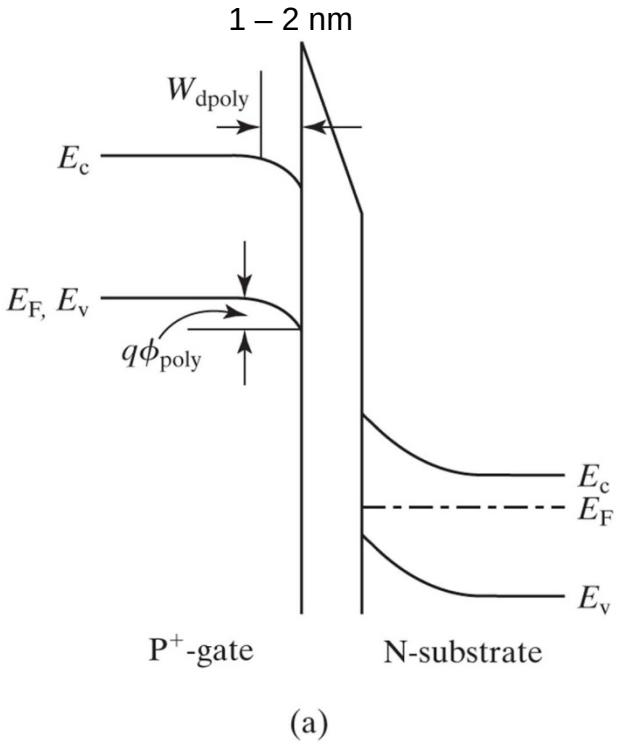
(a) without any oxide charge; (b) with Q_{ox} at the oxide–substrate interface.

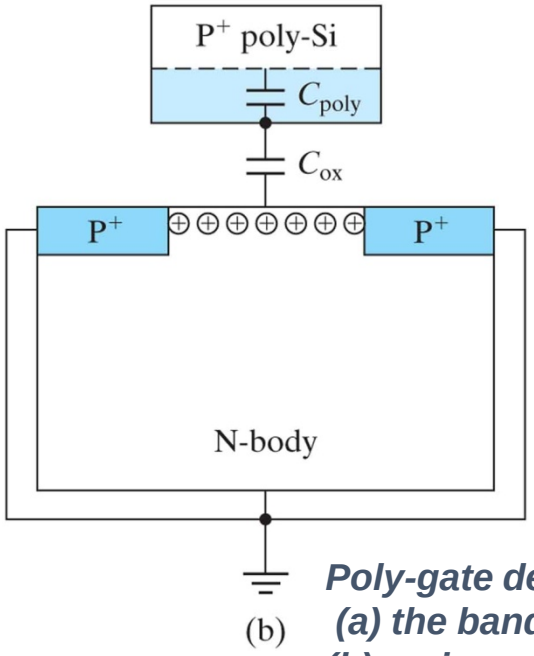
$$V_{fb0} = \psi_g - \psi_s$$

$$V_{fb} = V_{fb0} - \frac{Q_{ox}}{C_{ox}} = \psi_g - \psi_s - \frac{Q_{ox}}{C_{ox}}$$

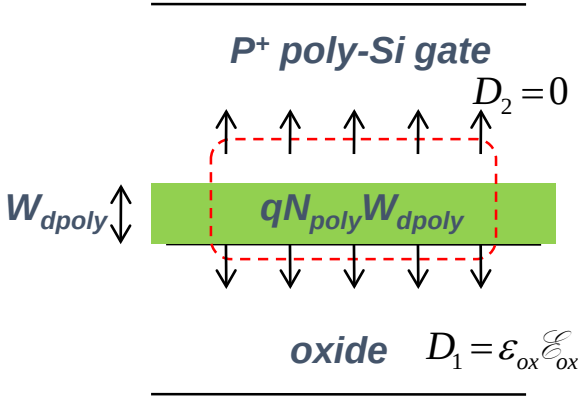
$$V_t = V_{fb} + 2\phi_B + \frac{\sqrt{qN_a 2\varepsilon_s 2\phi_B}}{C_{ox}}$$

Poly-Si Gate Depletion-Effective Increase in T_{ox}





Poly-gate depletion effect illustrated with (a) the band diagram and (b) series capacitors representation. An N+ poly-Si gate can also be depleted.



According to Gauss's Law,

$$D_1 + D_2 = -\varepsilon_{ox}\mathscr{E}_{ox} = -qN_{poly}W_{dpoly}$$

$$W_{dpoly} = \frac{\varepsilon_{ox}\mathscr{E}_{ox}}{qN_{poly}}$$

Poly-Si Gate Depletion-Effective Increase in T_{ox}

The MOS capacitance in the inversion region becomes

$$C = \left(\frac{1}{C_{ox}} + \frac{1}{C_{poly}} \right)^{-1} = \left(\frac{T_{ox}}{\varepsilon_{ox}} + \frac{W_{dpoly}}{\varepsilon_s} \right)^{-1} = \frac{\varepsilon_{ox}}{T_{ox} + W_{dpoly}/3}$$

Poly-depletion effect effectively increases T_{ox} by $W_{dpoly}/3$, and can have a significant impact on the C-V curve if T_{ox} is thin.

$$where \frac{\varepsilon_s}{\varepsilon_{ox}} \approx 3$$

Solutions; 1) dope the **poly-Si heavily** (can cause dopant penetration from the gate through the oxide into the substrate).
2) use **poly-SiGe gate** to be doped to a higher concentration.
3) substitute the poly-Si gate with **a metal gate.**

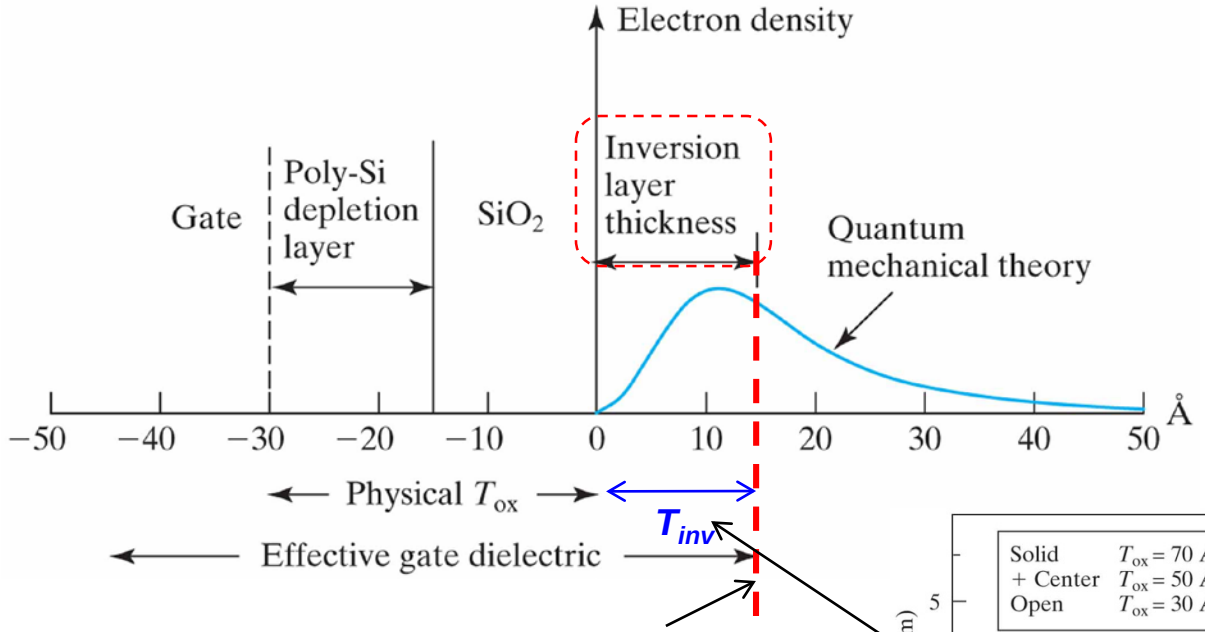
Poly-depletion effect is undesirable because a reduced C means reduced Q_{inv} and reduced transistor current.

$$Q_{inv} = -C_{ox}(V_g - \phi_{poly} - V_t)$$

Poly-gate depletion effectively reduces V_g by ϕ_{poly} .

Even 0.1 V ϕ_{poly} would be highly undesirable when the power-supply voltage is only around 1 V.

Inversion and Accumulation Charge-Layer Thicknesses and Quantum Mechanical Effect



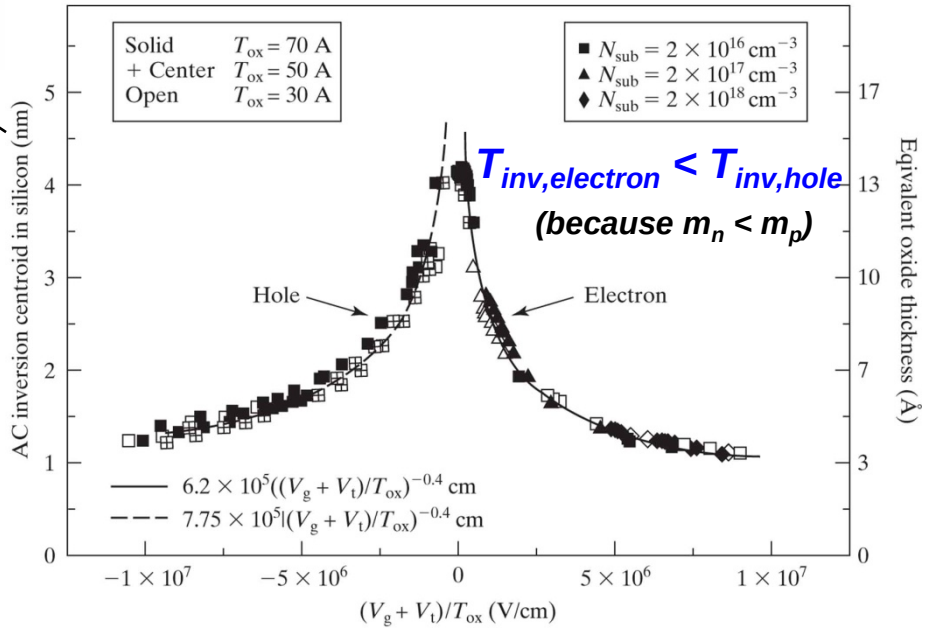
Effective bottom electrode of the MOS capacitor

$$Effective\ T_{ox} \approx T_{ox} + T_{inv}/3$$

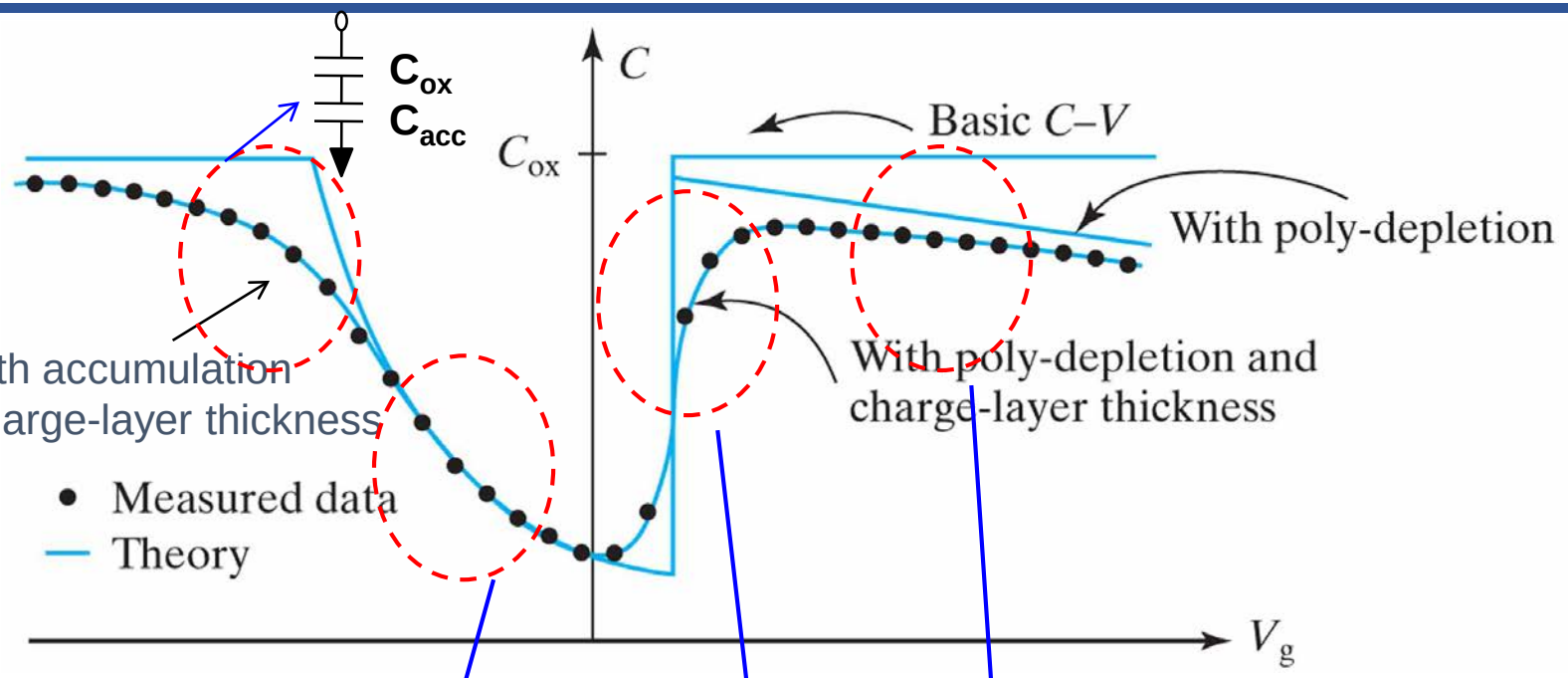
$$where\ 3 \approx \frac{\varepsilon_s}{\varepsilon_{ox}}$$

Average field in the inversion layer

$$= \frac{V_g + V_t}{6T_{ox}}$$

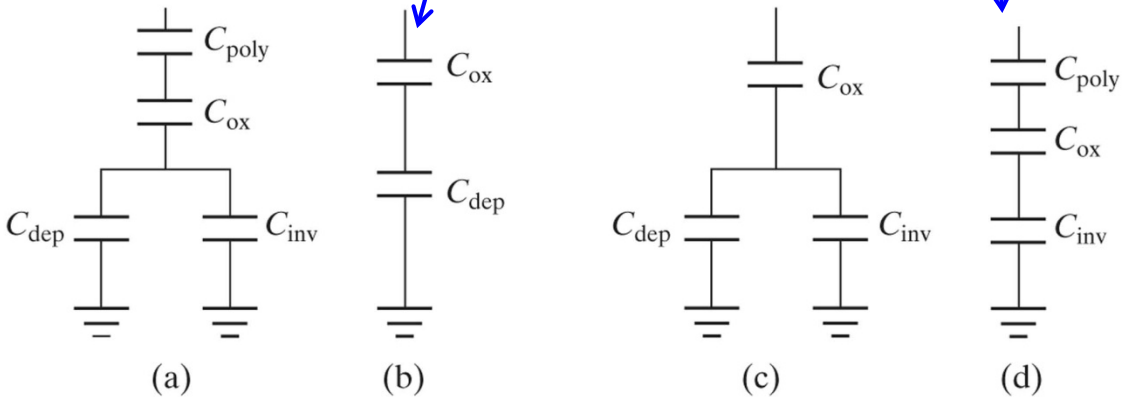


Average inversion-layer thickness (centroid) for electrons (in P body) and holes (in N body). (From [3]. © 1999 IEEE.)



The effects of poly-depletion and charge-layer thickness on the C–V curve of an N⁺ poly-gate, P-substrate device.

Increasing V_g.



Equivalent circuit for understanding the C–V curve in the depletion region and the inversion region. (a) General case for both depletion and inversion regions; (b) in the depletion regions; (c) $V_g \approx V_t$; (b) and (d) strong inversion.

Effective Oxide Thickness

- T_{inv} and W_{poly}: not negligible for thinner T_{ox} with thickness of < 10 nm
- Because it is difficult to separate T_{ox} from T_{inv} and W_{poly} by measurement, an **electrical oxide thickness, T_{oxe}**, is often used to characterize the total **effective oxide thickness.**
  (T_{oxe} is deduced from the inversion-region capacitance measured at $V_g = V_{dd}$.)
- **T_{oxe}** : an **effective oxide thickness** corresponding to an **effective gate capacitance, C_{oxe}.**

Total inversion charge per area, **Q_{inv}**, is

$$Q_{inv} = -C_{oxe}(V_g - V_t) = \frac{\varepsilon_{ox}}{T_{oxe}}(V_g - V_t)$$

$$T_{oxe} = T_{ox} + + W_{poly}/3 + T_{inv}/3 \qquad where \frac{\varepsilon_s}{\varepsilon_{ox}} \approx 3$$

Typically, T_{oxe} is larger than T_{ox} by 0.6-1.0 nm .

Quantum Effect on Threshold Voltage

At high substrate doping concentration, the high electric field in the substrate at the oxide interface causes energy levels to be quantized and effectively increases E_g and decreases n_i. This requires the band to bend down more before reaching threshold, i.e., causes ϕ_{st} to increase.

$$\phi_s = \phi_{st} = 2\phi_B = \frac{2kT}{q}\ln\frac{N_a}{n_i} \qquad V_t = V_{fb} + 2\phi_B + \frac{\sqrt{qN_a 2\varepsilon_s 2\phi_B}}{C_{ox}}$$

➡ The net effect is that the threshold voltage is increased by 100 mV or so depending on the doping concentration

CCD Imager and CMOS Imager

used in digital cameras and camcorders

- **CCD (Charge-Coupled Device) Imager:**
  1) high performance(good uniformity and contrast ratio)
  2) small number of sophisticated sensing circuits
  3) expensive.
- **CMOS Imager:**
  1) small area and less expensive
  2) compatible with CMOS IC technology
  3) easily integrated with signal processing and control circuits
  4) less power.

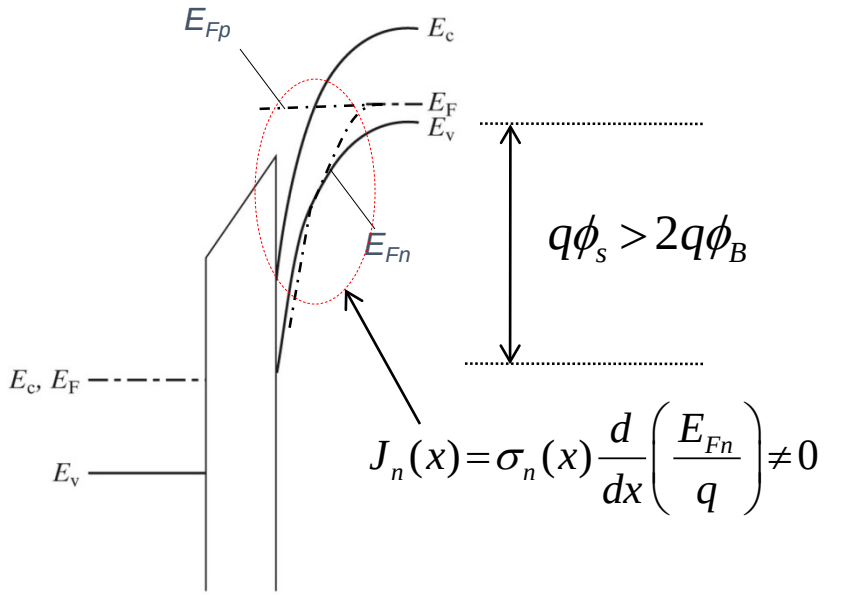
CCD Imager

The heart of a CCD imager is a large number of MOS capacitor densely packed in a two-dimensional array.

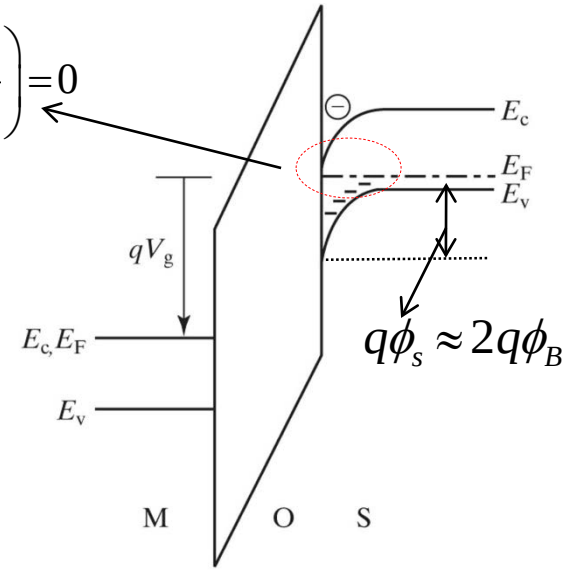
Deep Depletion

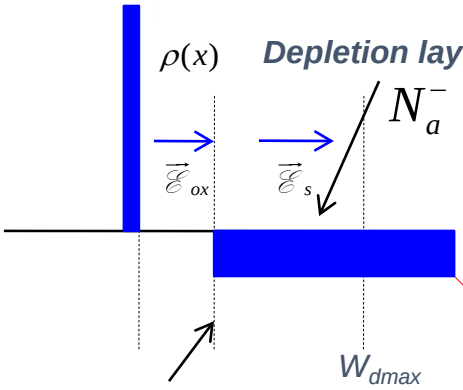
When a voltage, $V_g > V_t$, has been suddenly applied to the gate, an MOS capacitor is driven into nonequlibrium where *there are no electrons (no inversion layer) at the surface, because thermal generation is a slow process and,* in balancing the charge added to the gate, the depletion width becomes greater than W_{dmax} to offset the missing minority carriers. This called **"deep-depletion".**

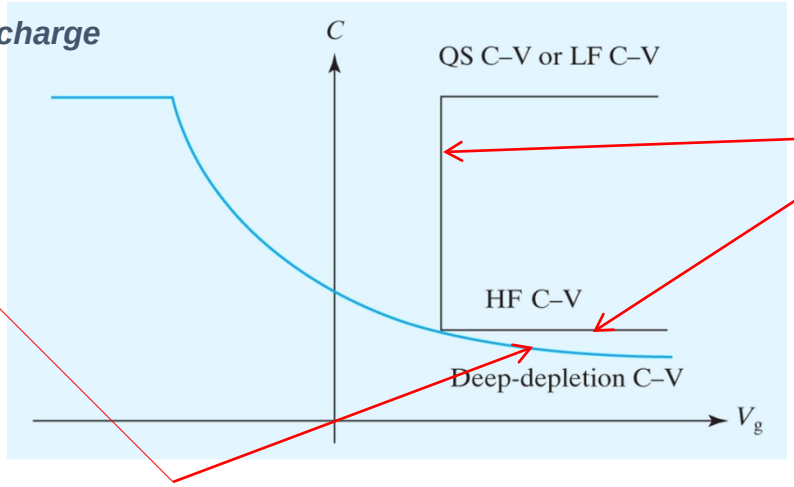
$$W_d > W_{d\max} \quad and \quad \phi_s > 2\phi_B$$

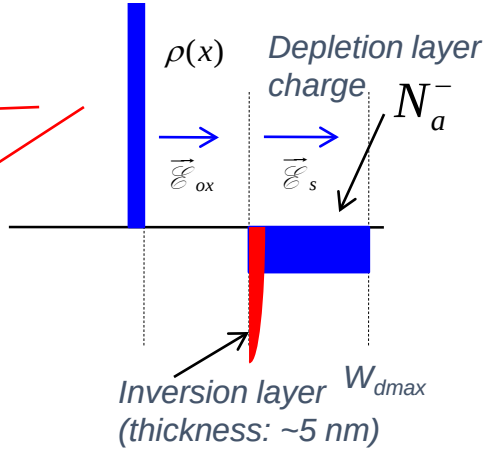


$$J_n(x) = \sigma_n(x)\frac{d}{dx}\left(\frac{E_{Fn}}{q}\right) = 0$$



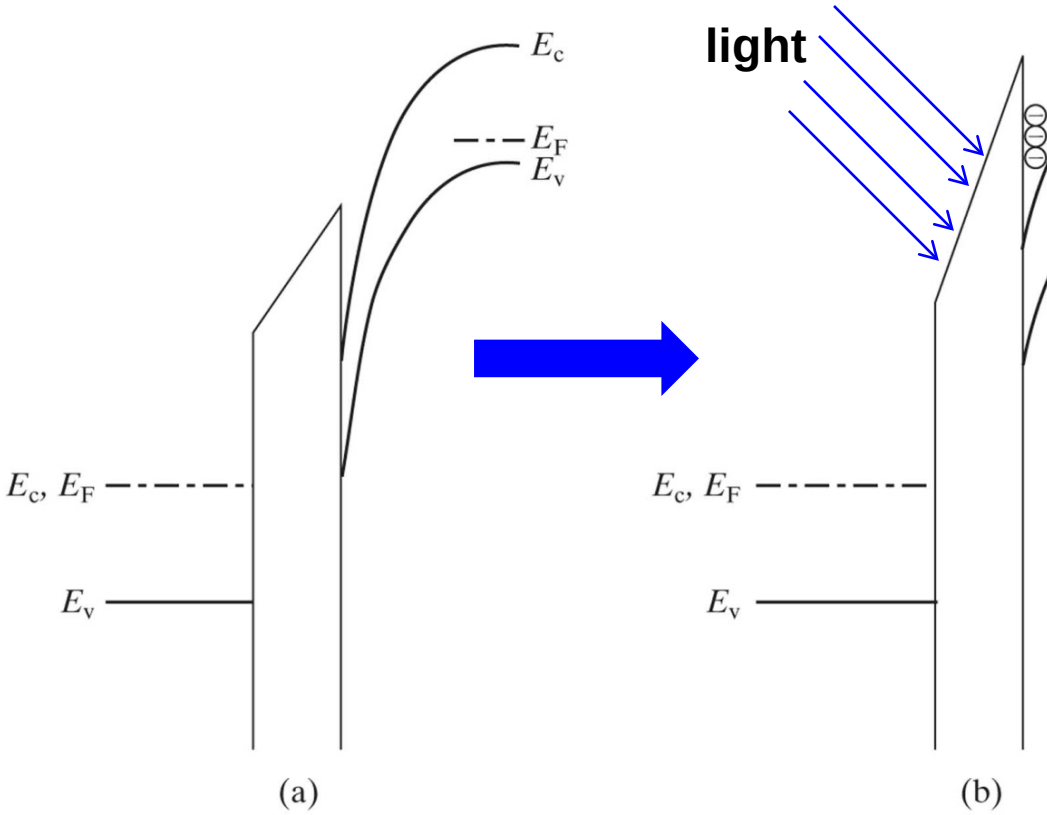






At nonequilibrium

Deep-depletion C–V
At equilibrium

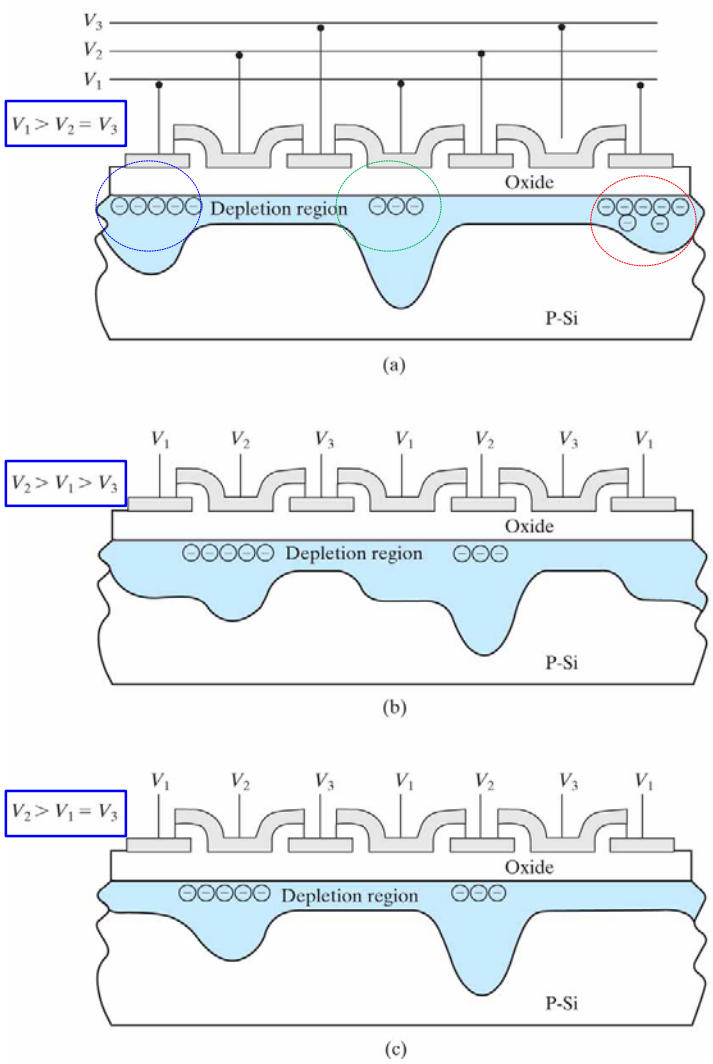


After exposure to light, photo-generated electrons have been collected at the surface. The number of electrons is proportional to the light intensity.

The first function of CCD array:
To convert an image(two-dimensional pattern of light intensity) into packets of electrons stored in a two-dimensional array of MOS capacitor

The second function of CCD array:
To transfer the collected charge packets to the edge of the array, where they can be read by a charge sensing circuit in a serial manner.

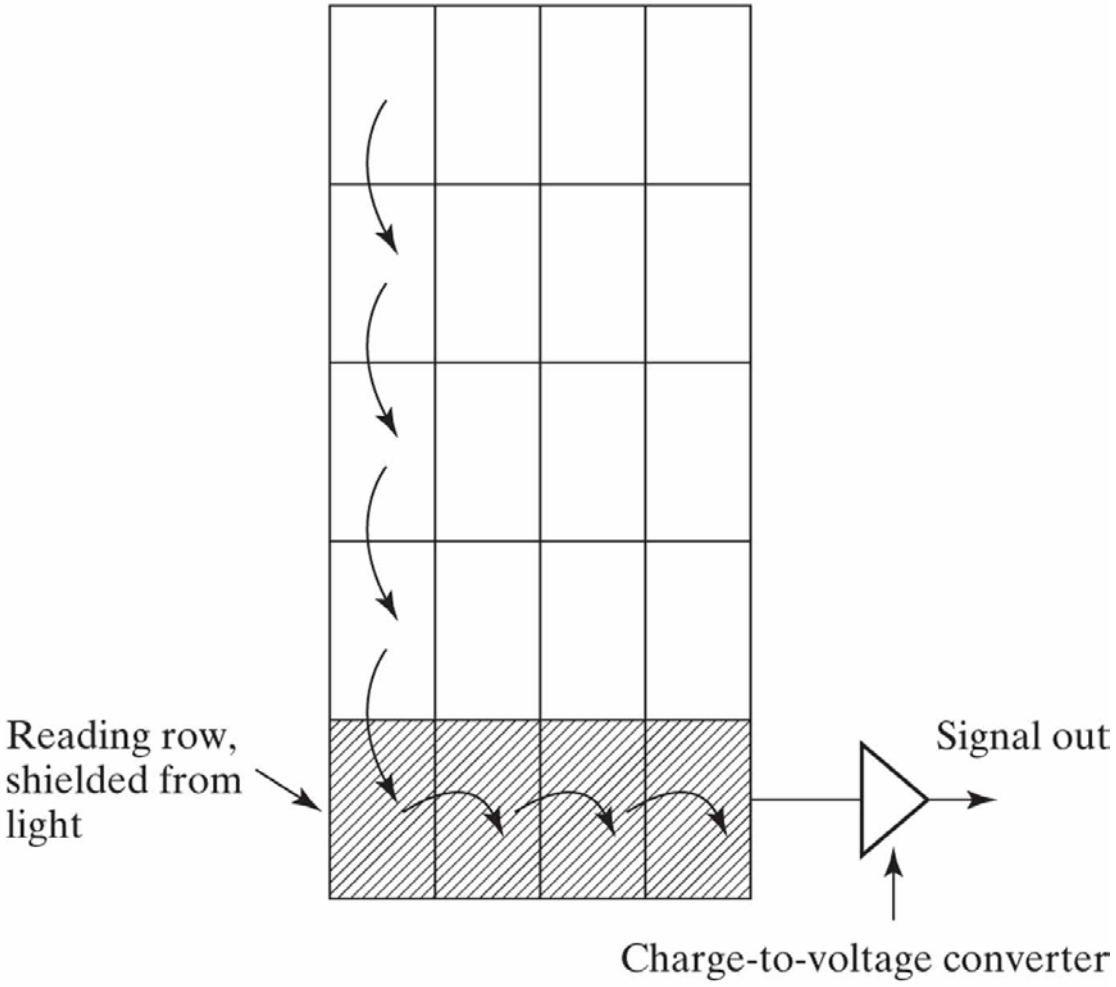
How does CCD shift the charge packets?



- **V_1 creates the deepest depletion.**
- Exposure to a lens-projected image has produced some electrons in the element on the right, even more in the element on the left and yet more in the middle element in proportion to the image light intensity around those three locations.
- **V_2 creates the deepest depletion.**
- The charge packets will move to the elements connected to V_2 (i.e., shifted to the right by one element. The choice of $V_1 > V_2$ ensures that no electrons are transferred to the left.
- **V_1 is reduced to the same values as V_3.**
  - The drawing in (c) is identical to (a) but with all the charge packets shifted to the right by one capacitor element.

The array is biased in the sequence (a), (b), (c), (a), (b), (c), (a) ... .
In this manner the electron packets are shifted to the right element by element.

Waiting at the right edge of the array is a **charge-sensing circuit** that generates a serial voltage signal that faithfully represents the image light pattern.

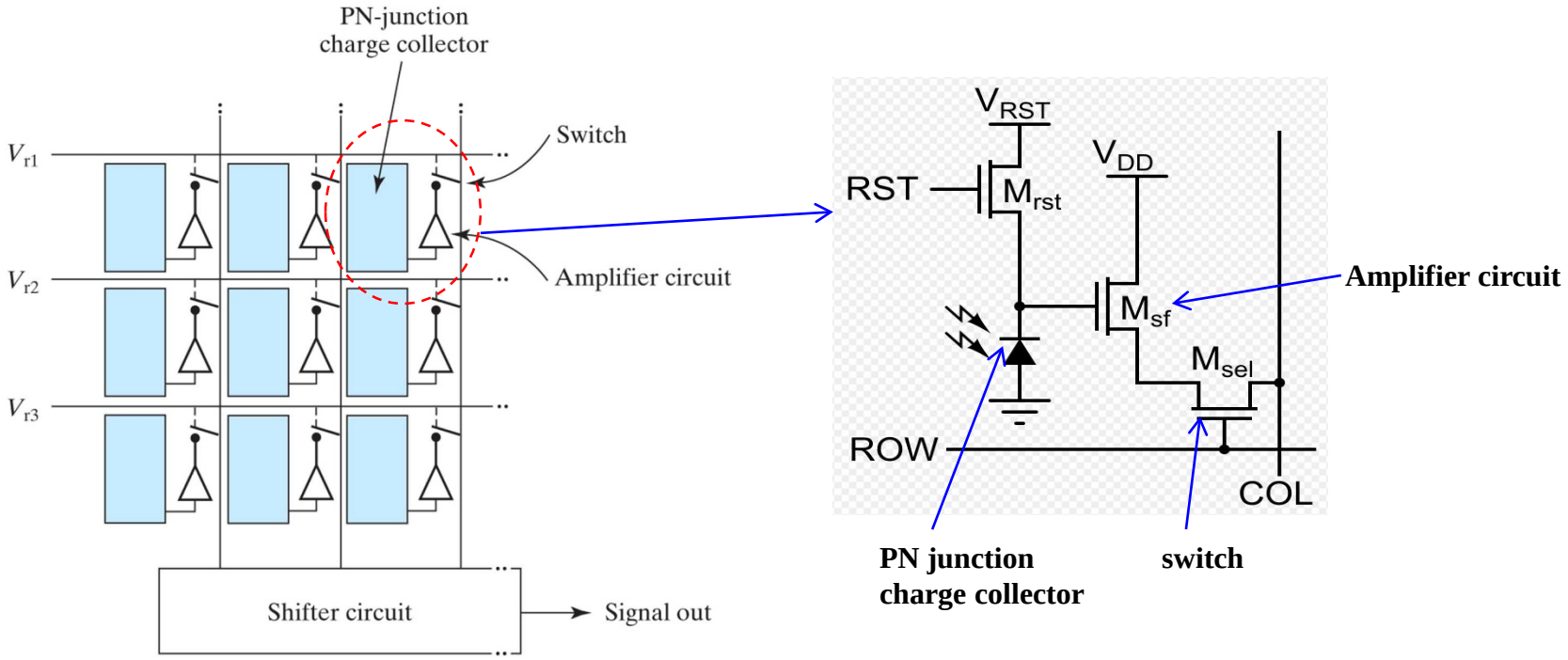


[Architecture of a two-dimensional CCD imager]
The arrows show the path of the charge-packet movement.

CMOS Imager

- Electrons generated by light near the PN junction diffuse to junction and get collected and stored in the thin N^+-region. Since the PN junction is a capacitor, the stored electrons change the capacitor voltage, i.e., the N^+-region voltage. This voltage is amplified in the pixel as shown in the figure below.

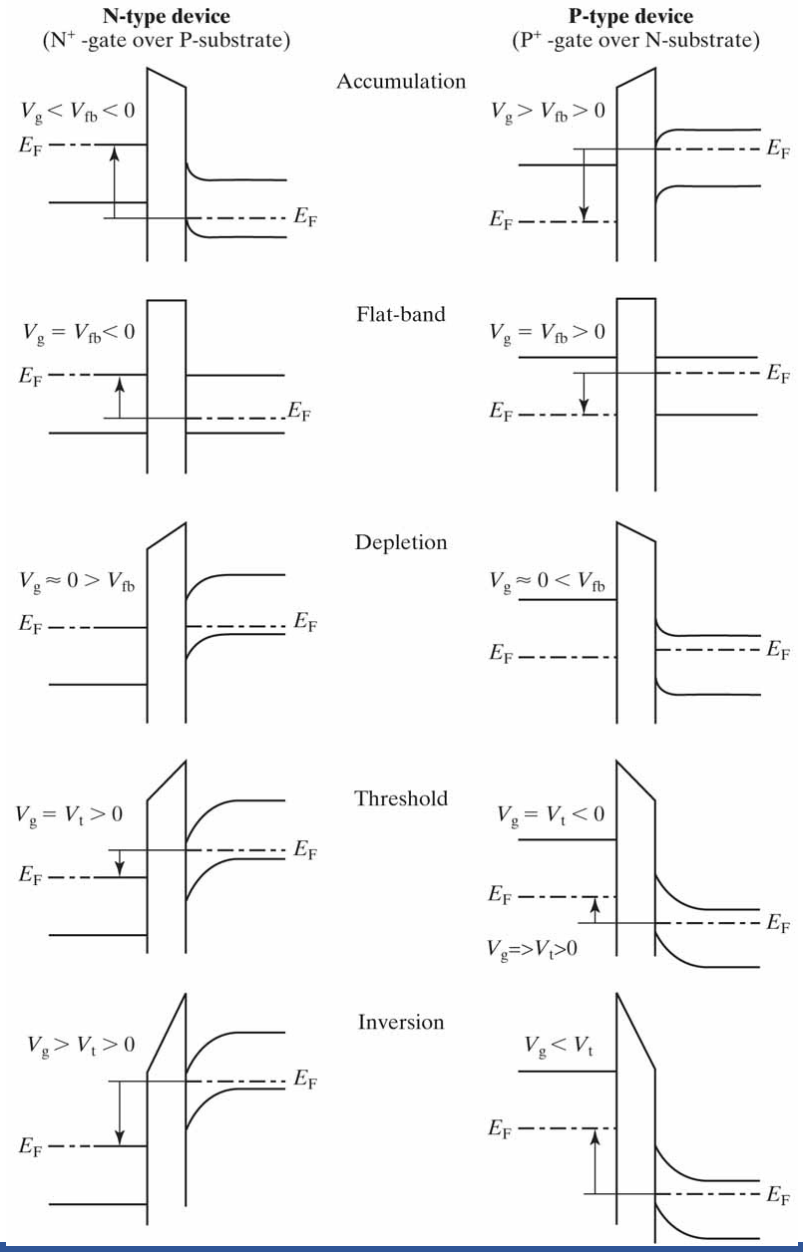
- Each pixel also contains a switch made of an MOS transistor and controlled by the voltage V_{r1}, V_{r2}, or V_{r3}. In order to read the top row of pixels, V_{r1} is raised to turn on (close) all the switches in the top row. This brings the signals from all the top-row pixels to the shifter circuit.



[Architecture of a CMOS imager]

Each array element has its own charge-to-voltage converter represented by the triangle. Actual imagers may support hundreds to over a thousand rows and columns of pixels.

Chapter Summary



Flat-band voltage

$$V_{fb} = \psi_g - \psi_s - Q_{ox} / C_{ox}$$

Gate voltage

$$V_g = V_{fb} + \phi_s + V_{ox} + \phi_{poly} = V_{fb} + \phi_s - Q_{sub} / C_{ox} + \phi_{poly}$$

Threshold voltage

$$V_t = V_g \Big|_{\phi_s = \phi_{st}} = V_{fb} + \phi_{st} + \frac{\sqrt{qN_{sub} 2\varepsilon_s |\phi_{st}|}}{C_{ox}}$$

$$\text{At threshold, } \phi_s = \phi_{st} = \pm 2\phi_B = \pm \frac{2kT}{q} \ln \frac{N_{sub}}{n_i}$$

Electrical oxide thickness

$$T_{oxe} = T_{ox} + + W_{poly} / 3 + T_{inv} / 3$$